TITLE **800G QSFP-DD AEC**	**DOC No. RFD-20230710003-001**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2023.07.07	**CLASSIFICATION：CONFIDENTIAL**

1. General Description

The P77003A00***-1 is a QSFP-DD to QSFP-DD active electrical cable for telecom and data center use, providing bi-directional 800G traffic per cable, 8 lanes of 100G PAM4. It adopts standard QSFP-DD type 2 form factor and complies with MSA specifications.

2. PRODUCT FEATURES

- Active Electrical Cable
- 8x100G PAM4 retimed
- 8x100G PAM4 retimed
- 800G to 800G data rate
- BER < 10^-6 (pre FEC)
- BER < 10^-15 (post FEC)
- Maximum link length of 3m
- Single 3.3V power supply
- Compliant with CMIS 5.2
- Hot pluggable
- Compliant with QSFP-DD MSA Rev 6.3
- Compliant with IEEE 802.3ck
- Power consumption less than 7.5W at each end
- Operating case temperature range of 0 to 70℃

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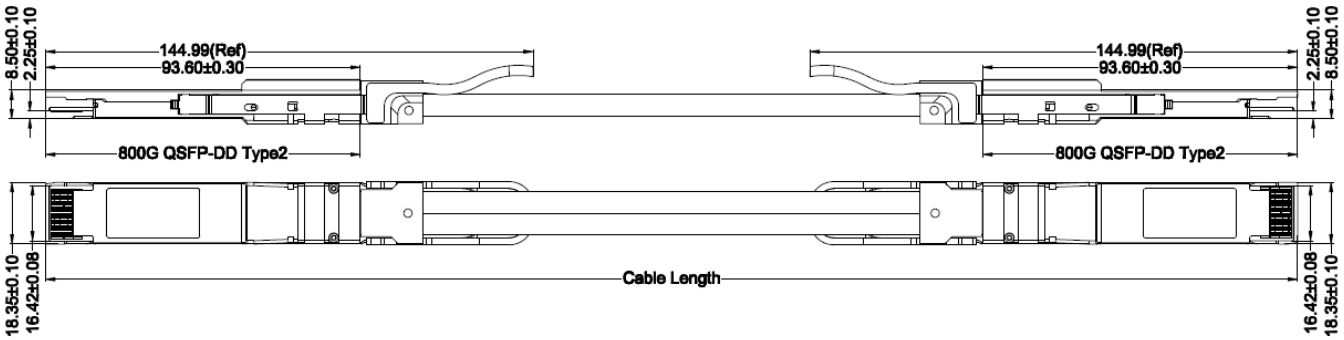
3. PRODUCT DESCRIPTION

3.1 PRODUCT NAME AND SERIES NUMBER(S)

800G QSFP-DD AEC

Part Number	Data Rate	Temp.	Distance	AWG
P77003A0001M-1	800G	C	1m	30
P77003A00150-1	800G	C	1.5m	30
P77003A0002M-1	800G	C	2m	30
P77003A00250-1	800G	C	2.5m	30
P77003A0003M-1	800G	C	3m	30

3.2 DIMENSIONS,MATERIALS,PLATINGS AND MARKING



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4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 800G Ethernet
- Date Center

5. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	℃
Case Operating Temperature	Top	0	70	℃
Relative Humidity(Non-condensing)	RH	5	85	%
Supply Voltage	VCC	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Top	0		70	℃
Power Supply Voltage	VCC	3.135		3.465	V
Total Power Consumption(each end)	Pc			7.5	W
Bit Rate	BR			850	Gbps

General Product Characteristics

Parameter	Min.	Typical	Max.	Unit	Note
Data rate per lane	53.125 ± 100ppm				PAM4
Differential input impedance	90	100	110	ohm	

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Differentialinput voltage amplitude	Pc	300	900	mV	
Common Mode to Differential Mode Conversion(SDC22)	Equation 23-2 OIF-CEI-112-VSR			dB	1
Differential Mode to Common Mode Conversion (SCD11)	Equation 23-1 OIF-CEI-112-VSR			dB	1
Common Mode Return Loss (SCC22)			-2	dB	
Common Mode Voltage (Vcm)	-350		2850	mV	2
Pre-FEC Bit Error Ratio			10^-6		3
Post-FEC Bit Error Ratio			10^-15		3
Module Form Factor		Type2			

Notes:

[1] S-parameter specifications are based on a differential reference impedance of 100 ohm and a common mode reference impedance of 25 ohm.

[2] Vcm is generated by the host. Specification includes effects of ground offset voltage.

[3] Tested with PRBS31Q pattern.

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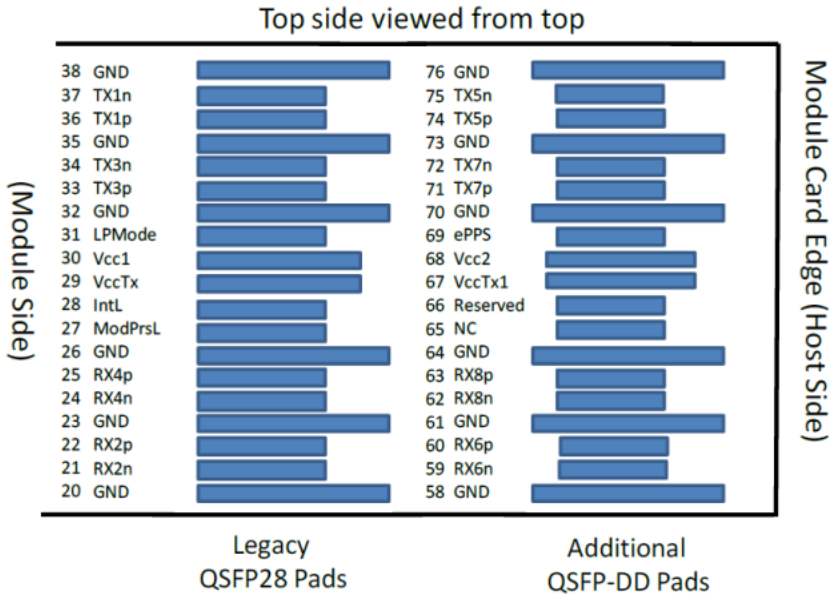
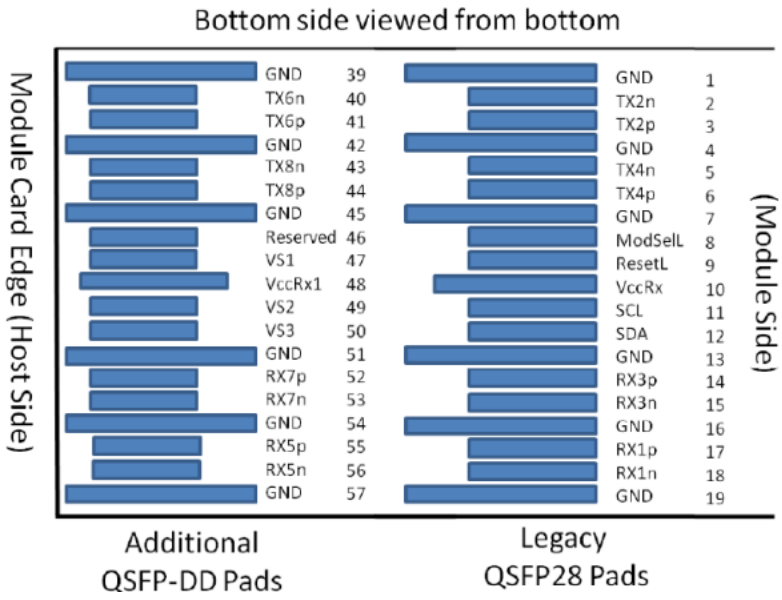
6. Pin-out Definition:

QSFP-DD AEC Pad Layout, host PCB QSFP-DD Pinout, and PIN Descriptions are as follows:





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Pin Assignment

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

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39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

[1] QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad

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65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B

7.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2023.07.07	Andy	Ray Yang